IN THE UNITED STATES DISTRICT COURT
FOR THE WESTERN DISTRICT OF TEXAS
AUSTIN DIVISION

VLSI TECHNOLOGY LLC,

Plaintiff,

v.

INTEL CORPORATION,

Defendant.

Civil Action No.: 1:19-cv-00977-ADA

INTEL'S STATEMENT REGARDING THE CONSTRUCTION OF "A CAPACITANCE STRUCTURE"

Defendant Intel Corporation ("Intel") hereby submits this Statement Regarding the Construction of "A Capacitance Structure" in response to the Court's request for a construction that represents the plain and ordinary meaning of the term in the context of the specification and prosecution history.[1]

U.S. Patent No. 7,292,485

'485 Patent		
Claim Term	**Intel's Construction**	**Intrinsic Support**
"a capacitance structure" (claims 1, 12, 17)	"a column or row of dummy memory cells"	"In another embodiment, the supply voltage is reduced during the write operation by charge sharing with ***a dummy column of memory cells***. The ***dummy column*** is implemented to be similar to a normal memory array column. The ***dummy column*** can be shared with any number of memory array columns. Charge sharing is decoded and is only applied on write cycles. Also, the amount of charge shared is programmable by selecting how many ***dummy cells*** are connected in ***the dummy column***. In another embodiment, the charge sharing is implemented using ***a dummy row***." '485 Patent

[1] Intel preserves its position that the term "a capacitance structure" is a means-plus-function term and should be construed pursuant to 35 U.S.C. § 112, ¶ 6.

'485 Patent		
Claim Term	**Intel's Construction**	**Intrinsic Support**
		at 2:13-23 (emphases added). "***Dummy column 17*** is similar to a normal memory column and includes a pair of dummy bit lines labeled 'SBL' and 'SBL*. ***Dummy SRAM cells 30, 32 and 34*** are coupled to the dummy bit lines SBL and SBL* and are conventional SRAM cells in the illustrated embodiment. Each of the ***dummy cells*** has a supply terminal that can be coupled to conductor 37…. ***Dummy column 17*** is used for capacitance sharing with memory array 14 during a write operation. The amount of capacitance shared is determined in part by how many ***memory cells*** are coupled to conductor 37." *Id.* at 3:59-4:7 (emphases added). "Charge sharing occurs between the selected columns of the memory array 14 and the ***dummy column 17*** to reduce the supply voltage of the memory cells of memory array 14 by a predetermined amount depending on the relative capacitances of ***dummy column 17*** and the selected columns of memory array 14. The capacitance of ***dummy column 17*** can be adjusted by selecting the number of ***memory cells*** coupled to conductor 37." *Id.* at 4:39-46 (emphases added). "***Dummy row 70*** is similar to a normal memory row and includes a word line labeled 'SWL' and all of the cells coupled to SWL. ***Dummy SRAM cells 82, 84, and 86*** are coupled to the dummy word line SWL and are conventional SRAM cells in the illustrated embodiment. Each of the ***dummy cells*** has a supply terminal that can be coupled to conductor 71…. ***Dummy row 70*** is used for capacitance sharing with memory array 14' during a write operation. The amount of capacitance shared is determined in part by how many ***memory cells*** are coupled to conductor 71." *Id.* at 5:39-57 (emphases added).

Dated: December 19, 2019

Respectfully submitted,

/s/ J. Stephen Ravel

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CERTIFICATE OF SERVICE

I hereby certify that all counsel of record who are deemed to have consented to electronic service are being served with a copy of the foregoing document via email on December 19, 2019.

/s/ J. Stephen Ravel
J. Stephen Ravel